CLAIMS

1. A high-speed digital transmitter capable of sending side channel data, the transmitter comprising:

a channel zero encoder having first and second inputs and an output, the first input receiving channel zero primary data, the second input receiving a channel zero DE_{out} signal, and the output producing channel zero encoded data, the channel zero encoder operative to produce channel zero encoded data based at least in part on the channel zero primary data and the channel zero DE_{out} signal;

a channel one multiplexer having at least first and second data inputs, at least one control input, and at least one output, the channel one multiplexer operative to multiplex channel one primary data and channel one side channel data, the first data input receiving channel one primary data, the second data input receiving channel one side channel data, the control input receiving a DEI signal, and the output providing a multiplexed signal including channel one side channel data and channel one primary data;

channel one DE_{out} control logic having a first input and an output, the channel one DE_{out} control logic operative to produce a channel one DE_{out} signal for facilitating the transfer of channel one side channel data, the first input receiving a DEI signal, and the output producing a channel one DE_{out} signal; and

a channel one encoder having first and second inputs and an output, the first input receiving the output of the channel one multiplexer, the second input

receiving the output of the channel one DE_{out} control logic, the output producing channel one encoded data, the channel one encoder operative to produce channel one encoded data based at least in part on the first and second inputs.

2. The transmitter of claim 1, wherein the channel zero DE_{out} signal is the DEI signal.

3. The transmitter of claim 1, wherein the channel zero encoder has third and fourth inputs for receiving Hsync and Vsync signals.

4. The transmitter of claim 1, wherein the transmitter further comprises:

a channel two multiplexer having at least first and second data inputs, a control input, and an output, the channel two multiplexer operative to multiplex channel two primary data and channel two side channel data, the first data input receiving channel two primary data, the second data input receiving channel two side channel data, the control input receiving a DEI signal, and the output providing channel two side channel data or channel two primary data depending on the value of the DEI signal;

channel two DE_{out} control logic having an input and an output, the channel two DE_{out} control logic operative to produce a channel two DE_{out} signal for facilitating the transfer of channel two side channel data, the first input receiving a DEI signal, and the output producing a channel two DE_{out} signal; and

a channel two encoder having first and second inputs and an output, the first input receiving the output of the channel two multiplexer, the second input receiving the output of the channel two DE_{out} control logic, the output producing channel two encoded data, the channel two encoder operative to produce channel two encoded data based at least in part on the first and second inputs.

5. The transmitter of claim 1, wherein the transmitter further comprises:

a channel one FIFO having an input for receiving channel one side channel data and an output coupled to the second data input of the channel one multiplexer, the output providing channel one side channel data to the channel one multiplexer.

6. The transmitter of claim 1, wherein the channel one encoder has third and forth inputs, the third input receiving a first control signal and the fourth input receiving a second control signal, and

wherein the channel one DE_{out} control logic has second and third inputs, the second input receiving the first control signal, and the third input receiving the second control signal.

7. The transmitter of claim 6, wherein the channel one DE_{out} control logic comprises:

a first control signal transition indication logic having an input and an output, the input adapted to receive the first control signal, the output providing a de-asserted signal as a result of a transition in the first control signal;

a second control signal transition indication logic having an input and an output, the input adapted to receive the second control signal, the output providing a de-asserted signal as a result of a transition in the second control signal;

DE_{out} inter-channel synchronization compliance logic having an input and an output, the input adapted to receive the DEI signal, the output providing a de-asserted period of a preselected length and at a preselected location relative to a de-asserted period in the DEI signal; and

An AND gate having first, second and third inputs and an output, the first input being coupled to the output of the first control signal transition indication logic, the second input being coupled to the output of the second control signal transition indication logic, the third input being coupled to the output of the DE_{out} inter-channel synchronization compliance logic, the output providing a digital visual interface compliant DE_{out} signal.

8. The transmitter of claim 7, wherein the first control signal transition indication logic comprises

a first delay element having an input and an output, the input adapted to receive the first control signal, the output producing a first delayed control signal;

a first logic gate having first and second inputs and an output, the first logic gate providing a de-asserted signal as a result of a transition of the first control signal, the first input coupled to the output of the first delay element, the second input adapted to receive the first control signal; and

wherein the second control signal transition indication logic comprises

a second delay element having an input and an output, the input adapted to receive the second control signal, the output producing a second delayed control signal;

a second logic gate having first and second inputs and an output, the second logic gate providing a de-asserted signal as a result of a transition of the second control signal, the first input coupled to the output of the second delay element, the second input adapted to receive the second control signal.

9. The transmitter of claim 7, wherein the channel one DEout control logic further comprises:

phase-tracking compliance logic having an input and an output, the input adapted to receive the DEI signal, the output providing a de-asserted signal as a result of a transition in the DEI signal.

10. The transmitter of claim 9, wherein the phase tracking compliance logic comprises:

a delay element having an input and an output, the input adapted to receive the DEI signal, the output producing a delayed DEI signal;

an inverter having an input and an output, the input adapted to receive the DEI signal, and the output producing an inverted DEI signal; and

a NAND gate having first and second inputs and an output, the first input coupled to the output of the delay element, the second input coupled to the output of the inverter, the output producing a low period as a result of a transition from high to low in the DEI signal.

11. A high-speed digital receiver capable of receiving side channel data, the receiver comprising:

a channel zero decoder having a first input and first and second outputs, the first input receiving channel zero encoded data, the first output producing a channel zero decoded data signal, the second output producing a channel zero DE_{out} signal, the channel zero decoder operative to produce channel zero decoded data and a channel zero DE_{out} signal from the channel zero encoded data;

a channel one decoder having at least an input and first and second outputs, the first input receiving channel one encoded data, the first output producing channel one decoded data, the second output producing a channel one DE_{out} signal, the channel one decoder operative to produce channel one decoded data and a channel one DE_{out} signal from the channel one encoded data;

DEI signal and FIFO control signal recovery logic having first and second inputs and first and second outputs, the first input receiving the channel zero DE_{out} signal, the second input receiving the channel one DE_{out} signal, the DEI signal and FIFO control signal recovery logic operative to derive a DEI signal, the first output producing a DEI signal, the second output producing a first FIFO control signal; and

a channel one de-multiplexer having a data input, a control input, and first and second outputs, the channel one de-multiplexer operative to separate channel one decoded data into channel one primary data and channel one

side channel data, the data input receiving channel one decoded data from the channel one decoder, the control input receiving the DEI signal from the DEI signal and FIFO control signal recovery logic, the first output producing channel one side channel data, and the second output producing channel one primary data.

12. The receiver of claim 11, wherein the receiver further comprises:

a channel two decoder having at least one input and at least first and second outputs, the first input receiving channel two encoded data, the first output producing channel two decoded data, the second output producing a channel two DE_{out} signal, the channel two decoder operative to produce channel two decoded data and a channel two DE_{out} signal from the channel two encoded data;

a channel two de-multiplexer having a data input, a control input, and first and second outputs, the channel two de-multiplexer operative to separate channel two decoded data into channel two primary data and channel two side channel data, the data input receiving channel two decoded data from the channel two decoder, the control input receiving the DEI signal from the DEI signal and FIFO control signal recovery logic, the first output producing channel two side channel data, and the second output producing channel two primary data.

13. The receiver of claim 12, wherein the DEI signal and FIFO control signal recovery logic comprises:

a first AND gate having first second and third inputs and an output, the first input adapted to receive the channel zero DE_{out} signal from the channel zero decoder, the second input adapted to receive the channel one DE_{out} signal from the channel one decoder, the third input adapted to receive the channel two DE_{out} signal from the channel two decoder, the output providing the DEI signal;

an inverter having an input and an output, the input coupled to the output of the first AND gate to receive the DEI signal, the output providing an inverted DEI signal;

a second AND gate having first and second inputs and an output, the first input coupled to the output of the inverter to receive the inverted DEI signal, the second input adapted to receive the channel one DE_{out} signal from the channel one decoder, the output providing a channel one FIFO control signal; and

a third AND gate having first and second inputs and an output, the first input coupled to the output of the inverter to receive the inverted DEI signal, the second input adapted to receive the channel two DE_{out} signal from the channel two decoder, the output providing a channel two FIFO control signal.

14. The receiver of claim 13, wherein the receiver further comprises:

a channel one FIFO having a data input, a control input and an output, the data input coupled to the first output of the channel one de-multiplexer, the control input adapted to receive the channel one FIFO control signal from

the second AND gate, and the output providing channel one side channel data; and

a channel two FIFO having a data input, a control input and an output, the data input coupled to the first output of the channel two de-multiplexer, the control input adapted to receive the channel two FIFO control signal from the third AND gate, and the output providing channel two side channel data.

15. A method for sending side channel data, the method comprising:

encoding channel zero primary data for transmission using a channel zero encoder having first and second inputs and one output, the first input receiving channel zero primary data, the second input receiving a channel zero DE_{out} signal, and the output producing channel zero encoded data, the channel zero encoder operative to produce channel zero encoded data based at least in part on the channel zero primary data and the channel zero DE_{out} signal;

multiplexing channel one primary data and channel one side channel data using a channel one multiplexer having first and second data inputs, a control input, and an output, the first data input receiving channel one primary data, the second data input receiving channel one side channel data, the control input receiving a DEI signal, and the output providing channel one side channel data or channel one primary data depending on the value of the DEI signal;

producing a channel one DEout signal for facilitating the transfer of channel one side channel data using channel one DE_{out} control logic having an input and an output, the first input receiving a DEI signal, and the output producing a channel one DE_{out} signal; and

encoding channel one data for transmission using a channel one encoder having first and second inputs and an output, the first input receiving the output of the channel one multiplexer, the second input receiving the output of the channel one DE_{out} control logic, the output producing channel one encoded data based at least in part on the two inputs.

16. A method for receiving side channel data, the method comprising:

receiving channel zero encoded data and channel one encoded data;

decoding channel zero encoded data using a channel zero decoder having a first input and first and second outputs, the first input receiving channel zero encoded data, the first output producing a channel zero decoded data signal, the second output producing a channel zero DE_{out} signal;

decoding channel one encoded data using a channel one decoder having at least an input and first and second outputs, the first input receiving channel one encoded data, the first output producing channel one decoded data, the second output producing a channel one DE_{out} signal;

deriving a DEI signal using DEI signal and FIFO control signal recovery logic having first and second inputs and first and second outputs, the first input receiving the channel zero DE_{out} signal, the second input receiving the

channel one DE_{out} signal, the first output producing a DEI signal, the second output producing a first FIFO control signal; and

separating channel one decoded data from channel one side channel data using a channel one de-multiplexer having a data input, a control input, and first and second outputs, the data input receiving channel one decoded data from the channel one decoder, the control input receiving the DEI signal from the DEI signal and FIFO control signal recovery logic, the first output producing channel one side channel data, and the second output producing channel one primary data.

17. A high speed digital transmission system capable of sending side channel, the system comprising:

a transmitter having first and second outputs,

a receiver having first and second inputs,

channel zero connecting the first output of the transmitter to the first input of the receiver, and

channel one connecting the second output of the transmitter to the second input of the receiver;

wherein the transmitter comprises:

a channel zero encoder having first and second inputs and an output, the first input receiving channel zero primary data, the second input receiving a channel zero DE_{out} signal, and the output producing channel zero encoded data, the channel zero encoder operative to

produce channel zero encoded data based at least in part on the channel zero primary data and the channel zero DE_{out} signal;

a channel one multiplexer having first and second data inputs, a control input, and an output, the channel one multiplexer operative to multiplex channel one primary data and channel one side channel data, the first data input receiving channel one primary data, the second data input receiving channel one side channel data, the control input receiving a DEI signal, and the output providing channel one side channel data or channel one primary data depending on the value of the DEI signal;

channel one DE_{out} control logic having an input and an output, the channel one DE_{out} control logic operative to produce a channel one DE_{out} signal for facilitating the transfer of channel one side channel data, the first input receiving a DEI signal, and the output producing a channel one DE_{out} signal; and

a channel one encoder having two inputs and one output, the first input receiving the output of the channel one multiplexer, the second input receiving the output of the channel one DE_{out} control logic, the output producing channel one encoded data the channel one encoder operative to produce channel one encoded data based at least in part on the two inputs; and

wherein the receiver comprises:

a channel zero decoder having an input and first and second outputs, the first input receiving channel zero encoded data, the first output producing a channel zero decoded data signal, the second output producing a channel zero DE_{out} signal, the channel zero decoder operative to produce channel zero decoded data and a channel zero DE_{out} signal from the channel zero encoded data;

a channel one decoder having at least one input and at least first and second outputs, the first input receiving channel one encoded data, the first output producing channel one decoded data, the second output producing a channel one DE_{out} signal, the channel one decoder operative to produce channel one decoded data and a channel one DE_{out} signal from the channel one encoded data;

DEI signal and FIFO control signal recovery logic having first and second inputs and first and second outputs, the first input receiving the channel zero DE_{out} signal, the second input receiving the channel one DE_{out} signal, the DEI signal and FIFO control signal recovery logic operative to derive a DEI signal, the first output producing a DEI signal, the second output producing a first FIFO control signal; and

a channel one de-multiplexer having a data input, a control input, and first and second outputs, the channel one de-multiplexer operative to separate channel one decoded data into channel one primary data and channel one side channel data, the data input receiving channel

one decoded data from the channel one decoder, the control input receiving the DEI signal from the DEI signal and FIFO control signal recovery logic, the first output producing channel one side channel data, and the second output producing channel one primary data.

18. A high-speed digital transmitter capable of sending side channel data, the transmitter comprising:

channel zero encoder means for producing channel zero encoded data, said channel zero encoder means having first and second inputs and an output, the first input receiving channel zero primary data, the second input receiving a channel zero DE_{out} signal, and the output producing channel zero encoded data based at least in part on the channel zero primary data and the channel zero DE_{out} signal;

channel one multiplexing means for multiplexing channel one primary data and channel one side channel data, said channel one multiplexing means having first and second data inputs, a control input, and an output, the first data input receiving channel one primary data, the second data input receiving channel one side channel data, the control input receiving a DEI signal, and the output providing channel one side channel data or channel one primary data depending on the value of the DEI signal;

channel one DE_{out} control logic means for producing a channel one DE_{out} signal for facilitating the transfer of channel one side channel data, said channel one DE_{out} control logic means having an input and an output, the first

input receiving a DEI signal, and the output producing a channel one DE_{out} signal; and

channel one encoding means for producing channel one encoded data, said channel one encoding means having first and second inputs and an output, the first input receiving the output of the channel one multiplexer, the second input receiving the output of the channel one DE_{out} control logic, the output producing channel one encoded data based at least in part on the two inputs.

19. The transmitter of claim 18, wherein the channel zero encoder means has third and fourth inputs for receiving Hsync and Vsync signals.

20. The transmitter of claim 18, wherein the transmitter further comprises:

a channel one FIFO having an input for receiving channel one side channel data and an output coupled to the second data input of the channel one multiplexing means, the output providing channel one side channel data to the multiplexing means.

21. A high-speed digital receiver capable of receiving side channel data, the receiver comprising:

channel zero decoder means for producing channel zero decoded data and a channel zero DE_{out} signal, said channel zero decoder means having an input and first and second outputs, the first input receiving channel zero encoded data, the first output producing a channel zero decoded data signal, the second output producing a channel zero DE_{out} signal;

channel one decoder means for producing channel one decoded data and a channel one DE_{out} signal, said channel one decoder means having at least one input and at least first and second outputs, the first input receiving channel one encoded data, the first output producing channel one decoded data, the second output producing a channel one DE_{out} signal;

DEI signal and FIFO control signal recovery logic means for deriving a DEI signal, said DEI signal and FIFO control signal recovery logic means having first and second inputs and first and second outputs, the first input receiving the channel zero DE_{out} signal, the second input receiving the channel one DE_{out} signal, the first output producing a DEI signal, the second output producing a first FIFO control signal; and

de-multiplexing means for separating a data signal into channel one primary data and channel one side channel data, said de-multiplexing means having a data input, a control input, and first and second outputs, the data input receiving channel one decoded data from the channel one decoder, the control input receiving the DEI signal from the DEI signal and FIFO control signal recovery logic, the first output producing channel one side channel data, and the second output producing channel one primary data.

22. A method for sending side channel data over a communication link having a transmitter, a receiver, and at least a channel zero and a channel one connecting the transmitter and the receiver, the method comprising:

encoding channel zero primary data, and DEI data as in-band and out-of-band characters for transmission on channel zero;

deriving a channel one DEout signal using channel one DE_{out} control logic having an input and an output, the first input receiving a DEI signal, and the output producing a channel one DE_{out} signal for facilitating the transfer of channel one side channel data;

encoding channel one primary data, channel one side channel data, and DE_{out} signal data for transmission on channel one, the encoding performed using in-band and out-of-band characters.

23. The method of claim 22, wherein the method further comprises:

selecting which channel will carry a substantially unaltered DE signal based on a characterization of the channels.

24. The method of claim 22, wherein the method further comprises:

communicating the capabilities of a receiver to a transmitter through a handshake procedure.

25. The method of claim 22, wherein deriving a channel one DEout signal comprises:

adjusting the length of a data inactive period within the channel one DEout signal based on a characterization of the channel.

26. A high-speed digital transmitter capable of sending side channel data, the transmitter comprising:

a channel zero encoder having first , second, third, and fourth inputs and an output, the first input receiving channel zero primary data, the second input receiving a DEI signal, the third input receiving an Hsync signal, the fourth input receiving a Vsync signal, and the output producing channel zero encoded data, the channel zero encoder operative to produce channel zero encoded data based at least in part on the channel zero primary data, the DEI signal, the Hsync signal, and the Vsync signal;

a channel one FIFO having an input for receiving channel one side channel data and an output for providing channel one side channel data;

a channel one multiplexer having at least first and second data inputs, at least one control input, and at least one output, the channel one multiplexer operative to multiplex channel one primary data and channel one side channel data, the first data input receiving channel one primary data, the second data input coupled to the output of the channel one FIFO for receiving channel one side channel data, the control input receiving a DEI signal, and the output providing a multiplexed signal including channel one side channel data and channel one primary data;

channel one DE_{out} control logic having a first input and an output, the channel one DE_{out} control logic operative to produce a channel one DE_{out} signal for facilitating the transfer of channel one side channel data, the first input receiving a DEI signal, and the output producing a channel one DE_{out} signal; and

a channel one encoder having first and second inputs and an output, the first input receiving the output of the channel one multiplexer, the second input receiving the output of the channel one DE_{out} control logic, the output producing channel one encoded data, the channel one encoder operative to produce channel one encoded data based at least in part on the first and second inputs.

27. A high-speed digital receiver capable of receiving side channel data, the receiver comprising:

a channel zero decoder having a first input and first and second outputs, the first input receiving channel zero encoded data, the first output producing a channel zero decoded data signal, the second output producing a channel zero DE_{out} signal, the channel zero decoder operative to produce channel zero decoded data and a channel zero DE_{out} signal from the channel zero encoded data;

a channel one decoder having at least an input and first and second outputs, the first input receiving channel one encoded data, the first output producing channel one decoded data, the second output producing a channel one DE_{out} signal, the channel one decoder operative to produce channel one decoded data and a channel one DE_{out} signal from the channel one encoded data;

DEI signal and FIFO control signal recovery logic having first and second inputs and first and second outputs, the first input receiving the channel zero DE_{out} signal, the second input receiving the channel one DE_{out} signal, the

DEI signal and FIFO control signal recovery logic operative to derive a DEI signal, the first output producing a DEI signal, the second output producing a first FIFO control signal; wherein the DEI signal and FIFO control signal recovery logic comprises:

a first AND gate having first second and third inputs and an output, the first input adapted to receive the channel zero DE_{out} signal from the channel zero decoder, the second input adapted to receive the channel one DE_{out} signal from the channel one decoder, the third input adapted to receive the channel two DE_{out} signal from the channel two decoder, the output providing the DEI signal;

an inverter having an input and an output, the input coupled to the output of the first AND gate to receive the DEI signal, the output providing an inverted DEI signal;

a second AND gate having first and second inputs and an output, the first input coupled to the output of the inverter to receive the inverted DEI signal, the second input adapted to receive the channel one DE_{out} signal from the channel one decoder, the output providing a channel one FIFO control signal; and

a third AND gate having first and second inputs and an output, the first input coupled to the output of the inverter to receive the inverted DEI signal, the second input adapted to receive the channel two DE_{out} signal from the channel two decoder, the output providing a channel two FIFO control signal, and

a channel one de-multiplexer having a data input, a control input, and first and second outputs, the channel one de-multiplexer operative to separate channel one decoded data into channel one primary data and channel one side channel data, the data input receiving channel one decoded data from the channel one decoder, the control input receiving the DEI signal from the DEI signal and FIFO control signal recovery logic, the first output producing channel one side channel data, and the second output producing channel one primary data.